

IN THE CLAIMS

Please amend the Claims as follows:

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1. (AMENDED) A method of forming dual damascene openings
in the fabrication of an integrated circuit device
comprising:
 providing metal lines covered by an insulating
 layer overlying a semiconductor substrate;
 5 depositing an organic dielectric layer overlying
 said insulating layer;
 depositing an inorganic dielectric layer overlying
 said organic dielectric layer wherein no etch stop layer
 10 is formed between said organic dielectric layer and said
 inorganic dielectric layer;
 etching a via pattern into said inorganic
 dielectric layer;
 etching said via pattern into said organic
 15 dielectric layer using patterned said inorganic
 dielectric layer as a mask; and
 thereafter etching a trench pattern into said
 inorganic dielectric layer to complete said forming of
 said dual damascene openings in the fabrication of said
 20 integrated circuit device.

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3. (AMENDED) The method according to Claim 1 wherein
said organic dielectric layer comprises polyimides,
HOSP, SILK, FLARE, benzocyclobutene (BCB),
methylsilsesquioxane (MSQ), or organic polymers.

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4. (AMENDED) The method according to Claim 1 wherein
said inorganic dielectric layer comprises CORAL, BLACK
DIAMOND, fluorinated silicate glass (FSG), carbon-doped
FSG, nitrogen-doped FSG, Z3MS, XLK, or hydrogen
silsesquioxane (HSQ).

6. (AMENDED) A method of forming dual damascene openings
in the fabrication of an integrated circuit device
comprising:

5 providing metal lines covered by an insulating
layer overlying a semiconductor substrate;
 depositing an organic dielectric layer overlying
said insulating layer;
 depositing an inorganic dielectric layer overlying
said organic dielectric layer wherein no etch stop layer
10 is formed between said organic dielectric layer and said
inorganic dielectric layer;
 etching a trench pattern into said inorganic
dielectric layer; and
 thereafter etching a via pattern through said

15 inorganic dielectric layer and said organic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

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8. (AMENDED) The method according to Claim 6 wherein said organic dielectric layer comprises polyimides, HOSPI, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), or organic polymers.

9. (AMENDED) The method according to Claim 6 wherein said inorganic dielectric layer comprises CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, or hydrogen silsesquioxane (HSQ).

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11. (AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an organic dielectric layer overlying said insulating layer;

depositing an inorganic dielectric layer overlying said organic dielectric layer wherein no etch stop layer

10 is formed between said organic dielectric layer and said inorganic dielectric layer;

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etching a via pattern into said inorganic dielectric layer; and

15 simultaneously etching said via pattern into said organic dielectric layer and etching a trench pattern into said inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

13. (AMENDED) The method according to Claim 11 wherein said organic dielectric layer comprises polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), or organic polymers.

14. (AMENDED) The method according to Claim 11 wherein said inorganic dielectric layer comprises CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, or hydrogen silsesquioxane (HSQ).

16. (AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

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providing metal lines covered by an insulating

5 layer overlying a semiconductor substrate;
 depositing an inorganic dielectric layer overlying
 said insulating layer;
 depositing an organic dielectric layer overlying
 said inorganic dielectric layer wherein no etch stop
10 layer is formed between said inorganic dielectric layer
 and said organic dielectric layer;
 etching a via pattern into said organic dielectric
 layer;
 etching said via pattern into said inorganic
15 dielectric layer using patterned said organic dielectric
 layer as a mask; and
 thereafter etching a trench pattern into said
 organic dielectric layer to complete said forming of
 said dual damascene openings in the fabrication of said
20 integrated circuit device.

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18. (AMENDED) The method according to Claim 16 wherein
 said inorganic dielectric layer comprises CORAL, BLACK
 DIAMOND, fluorinated silicate glass (FSG), carbon-doped
 FSG, nitrogen-doped FSG, Z3MS, XLK, or hydrogen
 silsesquioxane (HSQ).

19. (AMENDED) The method according to Claim 16 wherein
 said organic dielectric layer comprises polyimides,

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HOSP, SILK, FLARE, benzocyclobutene (BCB),
methylsilsesquioxane (MSQ), or organic polymers.

21. (AMENDED) A method of forming dual damascene
openings in the fabrication of an integrated circuit
device comprising:

providing metal lines covered by an insulating
5 layer overlying a semiconductor substrate;

depositing an inorganic dielectric layer overlying
said insulating layer;

depositing an organic dielectric layer overlying
said inorganic dielectric layer wherein no etch stop
10 layer is formed between said inorganic dielectric layer
and said organic dielectric layer;

etching a trench pattern into said organic
dielectric layer; and

thereafter etching a via pattern through said
15 organic dielectric layer and said inorganic dielectric
layer to complete said forming of said dual damascene
openings in the fabrication of said integrated circuit
device.

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23. (AMENDED) The method according to Claim 21 wherein
said inorganic dielectric layer comprises CORAL, BLACK
DIAMOND, fluorinated silicate glass (FSG), carbon-doped

FSG, nitrogen-doped FSG, Z3MS, XLK, or hydrogen silsesquioxane (HSQ).

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24. (AMENDED) The method according to Claim 21 wherein said organic dielectric layer comprises polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), or organic polymers.

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26. (AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating
5 layer overlying a semiconductor substrate;
depositing an inorganic dielectric layer overlying
said insulating layer;
depositing an organic dielectric layer overlying
said inorganic dielectric layer wherein no etch stop
10 layer is formed between said inorganic dielectric layer
and said organic dielectric layer;
etching a via pattern into said organic dielectric
layer; and
simultaneously etching said via pattern into said
15 inorganic dielectric layer and etching a trench pattern
into said organic dielectric layer to complete said
forming of said dual damascene openings in the